In The Specification

Please replace paragraph 001 with the following re-written paragraph:

001 This invention generally relates to semiconductor processing and more particularly to thermal degradation of photoresist layers included~~ing~~ ~~on~~ in flip chip bonding technology and a method for preventing the formation of difficult to remove photoresist residue on a semiconductor process wafer surface following a thermal treatment.

Please replace paragraph 004 with the following re-written paragraph:

004 In many cases it is necessary to repackage the chip after a package failure requiring costly detachment of the chip from the package and repeating the chip bonding process in a new package. Some chip bonding technologies utilize a solder bump attached to a contact pad (chip bonding pad) on the chip to make an electrical connection from the chip devices to the package. For example, C4 (Controlled-Collapse Chip Connection) is a means of connecting semiconductor chips to substrates in electronic packages. C4 is a flip-chip technology in which the

interconnections are small solder balls (bumps) on the chip surface. Since the solder balls form[s] an area array, C4 technology can achieve the highest density scheme known in the art for chip interconnections. The flip chip method has the advantage of achieving the highest density of interconnections to the device with the lowest parasitic inductance.

Please replace paragraph 007 with the following re-written paragraph:

007 If the column of solder material is inhomogeneous, for example, solder paste applied using the photoresist layer 16 as a stencil (stencil printing), then prior to removal of the photoresist layer 16, a first reflow process is typically performed to harden the printed solder paste and form a homogeneous column (plug) of solder material confined by the photoresist layer 16 stencil in preparation for a second reflow process for forming a solder ball carried out after removing the photoresist layer 16. After removal of the photoresist layer 16, the UBM layer 14A is typically etched through by a reactive ion etch (RIE) process to the underlying passivation layer 12 using the solder column 18A as an etching mask to protect the underlying UBM layers e.g., 14A, 14B, and 14C, as shown in Figure 1D. The solder column 18 is then heated to reflow to form a

solder bump 18B over the UBM layer 14C as shown in Figure 1E. After reflow, a homogeneous Pb/Sn solder bump is formed including, for example, with composition ratios indicating weight percent, high lead alloys including 95 Pb/5 Sn (95/5) or 90 Pb/10 Sn (950/10) with melting temperatures, for example, in excess of 350 °C. The solder bump forms a homogeneous material and has a well defined melting temperature. The lead content (high melting) Pb/Sn alloys are reliable bump metallurgies which are particularly resistant to material fatigue.

Please replace paragraph 0010 with the following re-written paragraph:

0010 It is therefore an object of the invention to provide ~~to develop~~ an improved process whereby thermal degradation of a photoresist layer in contact with a semiconductor process wafer surface during a thermal treatment, including solder reflow, is avoided thereby eliminating the deposition of a thermally degraded photoresist residue to provide for a clean semiconductor process wafer surface allowing more reliable subsequent processing steps, while overcoming other shortcomings and limitations of the prior art.

Please replace paragraph 0029 with the following re-written paragraph:

0029 According to the present invention a protective layer 24C of organic material, for example, Benzocyclobutene (BCĐB), having a glass transition temperature (Tg) about greater than a thermal treatment temperature, for example 350 °C, is deposited over the first layer of photoresist 24B to include deposition over exposed ~~UBM layer 24A (contact layer)~~ portions of passivation layer 22 as shown in Figure 2D. Preferably, the protective layer 24C is applied by a conventional spin coating process. The protective layer 24C is preferably an organic resinous material that can withstand thermal degradation at temperatures at least greater than about 300°C. For example, a suitable organic resinous material includes BCĐB having a glass transition temperature Tg of greater than about 350°C. For example, a resinous organic material that has suitable thermal stability at temperatures greater than about 350°C is CYCLOTENE™ 4026-46, a Benzocyclobutene (BCĐB) commercially available from DOW Chemical.

Please replace paragraph 0033 with the following re-written paragraph:

0033 After reflow, a homogeneous Pb/Sn solder column is formed including, for example, with composition ratios indicating weight percent, high lead alloys including 95 Pb/5 Sn (95/5) or 90 Pb/10 Sn (950/10) with melting temperatures in excess of 300°C.